REMARKS

Applicant respectfully requests re-consideration of the application in view of the arguments presented below.

Summary of Office Action

Claims 1-20 are pending.

Claims 11-20 were allowed.

Claims 1 and 8 were rejected under 35 U.S.C. § 102 as being anticipated by U.S. Patent No. 5,689,259 of Ozguc ("Ozguc").

Claim 6 was rejected under 35 U.S.C. § 103 as being unpatentable over U.S. Patent No. 6,426,715 of Westra, et al. ("Westra").

Claims 2-5, 7, 9, and 10 were indicated as being allowable if re-written.

Response to 35 U.S.C. § 102 rejections

Claims 1 and 8 were rejected as being anticipated by Ozguc. *Applicant respectfully submits that Ozguc does not teach or suggest a) first and second current steering DAC; b) each having a differential output; or c) switch circuitry that couples the differential output of a selected DAC to a pair of switch nodes while shorting the differential output of the other DAC.*

The Examiner has stated in part:

> Ozguc discloses an apparatus for performing digital-to-analog conversion, comprising: first and second current steering digital-to-analog converters (12,14), each DAC having a first and second output (D5 and BarD5) forming a differential DAC output (OUTP, OUTN).

(06/25/2004 Office Action, p. 2)

Applicant respectfully traverses the Examiner's characterization of Ozguc. With respect to applicant's point (a), *there is no teaching or suggestion that Ozguc's DACs are current steering DACs.* The Examiner is referred to Ozguc's detailed DAC schematic illustrated in Figure 2.

With respect to applicant's point (b), although Ozguc's OUTP and OUTN may represent a differential signal, each DAC 12, 14 provides a single-ended (i.e., not a differential) output.

The Examiner has incorrectly identified D5 and $\overline{D5}$ as the outputs of the DACs. *Clearly,* D5 and $\overline{D5}$ *are not the DAC outputs,* they are the control signals for the switch circuitry 18, 22, 26, 28 used to cross-couple the DACs 12, 14 to output nodes OUTP and OUTN. D5 is actually one bit of the 6 bit DAC *input* D0-D5. (Ozguc, col. 2, lines 36-50). DAC 12 provides the same single-ended output signal to both switch 18 and switch 26 as evidenced by the connection node appearing just to the left of switch 18 in Ozguc's Figure 1A. Similarly, DAC 14 is providing the same single-ended output signal to both switch 28 and switch 22 as evidenced by the connection node appearing just to the left of switch 22 in Ozguc's Figure 1A. Signals D5 and $\overline{D5}$ are used to toggle the single output of each DAC to one of two output nodes OUTP or OUTN. (Ozguc, Fig. 1A). Neither DAC 12 nor DAC 14 of Ozguc provides a differential output signal. *Thus Ozguc does not teach or suggest first and second DACs, each DAC having a first and second output forming a differential DAC output.*

With respect to applicant's point (c), applicant again notes that each of Ozguc's DACs have a single-ended output. The cross-coupled switch circuitry

operates to connect a selected DAC output to OUTP. The other DAC output is connected to OUTN. Each DAC is always exclusively connected to one of the two switch nodes by the cross-coupled switch circuitry in accordance with the value of D5. Neither DAC has its output shorted with itself, to ground, or to Vref (i.e., the common node) at any time.

The Examiner has stated in part:

> ...wherein the differential output of a non-selected one of the first and second DACs is shorted (Fig. 1 and 2 disclosing the non-selecting differential output D5 and BarD5 of DAC 12 and DAC 14 is shorted on a common line output of each ADC).

(6/25/2004 Office Action, p. 2-3)

Applicant is unable to reasonably interpret the Examiner's comment and respectfully requests clarification. The Examiner seems to be admitting that neither DAC provides a differential output signal ("common line output of each ADC"), but D5 and "BarD5" are not DAC outputs.

Signals D5 and $\overline{D5}$ are used to toggle switches to route the single output of each DAC mutually exclusively to one of two output nodes OUTP or OUTN. Ozguc's DACs convert a 6-bit code represented by D0-D5. The last bit, D5, is used to control four switches that connect the outputs of the DACs in cross-coupled fashion. (Ozguc, col. 2, lines 36-50; col. 3, lines 33-39, Fig. 1A, 2). *D5 is clearly a DAC input - not a DAC output as alleged by the Examiner.* The value of D5 input determines which DAC is coupled to OUTP and which DAC is coupled to OUTN. A DAC is either coupled to OUTP or OUTN. There is no teaching or suggestion of grounding any DAC output. (The Vref applied to each DAC is not

a DAC output. Vref is a DAC reference voltage, see, e.g., Ozguc, col. 1 lines 46-50, col. 3, lines 6-33, 53-59; Fig. 1A, 2).

If neither DAC has a differential output, then Ozguc cannot teach switch circuitry coupling such a differential output nor shorting such a differential output. Accordingly, *applicant submits Ozguc does not teach or suggest switch circuitry that couples the differential output of a selected DAC to a pair of switch nodes while shorting the differential output of the other DAC.*

Thus applicant respectfully submits Ozguc does not teach or suggest ANY of the following elements: *a) first and second current steering DACs; b) each having a differential output; or c) switch circuitry that couples the differential output of a selected DAC to a pair of switch nodes while shorting the differential output of the other DAC.*

In contrast, claim 1 includes the language:

> 1. An apparatus for performing digital-to-analog conversion, comprising:
> *first and second current steering digital-to-analog converters (DAC), each DAC having a first and second output forming a differential DAC output;* and
> *switch circuitry, wherein the switch circuitry couples the differential output of at most a selected one of the first and second DACs to a pair of switch nodes, wherein the differential output of a non-selected one of the first and second DACs is shorted.*

(Claim 1)(*emphasis added*)

Thus applicant submits claim 1 is not anticipated under 35 U.S.C. § 102 by Ozguc. Given that claims 2-10 depend from claim 1, applicant submits claims 2-10 are likewise not anticipated by Ozguc.

Applicant respectfully submits the rejections under 35 U.S.C. § 102 have been overcome.

Response to 35 U.S.C. § 103 rejections

Claim 6 was rejected under 35 U.S.C. § 103 as being unpatentable over Ozguc in view of Westra. The Examiner incorporated a differential amplifier taught by Westra's DAC into Ozguc's DAC for the stated purpose of providing a differential analog output voltage signal. Applicant notes that no 35 U.S.C. § 103 rejection was applied to the independent claim 1 from which claim 6 depends.

Applicant questions the Examiner's stated motivation. As stated previously Ozguc's overall circuitry provided a differential output but the individual DACs are single-ended rather than differential output devices. The Examiner's stated motivation seems to suggest that the Examiner is either a) agreeing that Ozguc's individual DACs are not differential output devices OR alternatively b) that Ozguc's overall circuit does not provide a differential output? Applicant has difficulty reconciling either interpretation with the Examiner's earlier characterization of Ozguc.

With respect to alternative a), the Examiner previously argued that each of Ozguc's DACs provided a differential output. Applicant previously disputed this point. Applicant is uncertain whether the Examiner is now taking a position contrary to the Examiner's own earlier characterization of Ozguc?

With respect to alternative b), applicant notes that Ozguc's overall circuitry already provides a differential output at nodes OUTP and OUTN. Accordingly, there would be no need to contribute a differential amplifier for the purpose of providing a differential analog output voltage when such an output voltage is already provided.

Regardless of the proper interpretation of the Examiner's remarks, applicant notes that none of the Examiner's cited references, alone or in combination, teaches or suggests *switch circuitry coupling the differential output of at most a selected one of the first and second DACs to a pair of switch nodes*, wherein the differential output of a non-selected one of the first and second DACs is shorted.

As previously noted, Ozguc's DACs are single-ended rather than differential output DACs. Moreover, the output of each DAC is always coupled to one of the two output nodes OUTP, OUTN such that there are always two DACs having an output coupled to the pair of switch nodes - one DAC output to each node. Ozguc does not teach or suggest *switch circuitry coupling the differential output of at most a selected one of the first and second DACs to a pair of switch nodes* as previously argued above with respect to the 35 U.S.C. § 102 rejections.

Westra's Figures 1 and 3 illustrates a pair of DACs each DAC having a plurality of output lines. One output line from each DAC is connected to a common ground. Each of the remaining output line(s) of one DAC are connected to corresponding complementary output line(s) of the other DAC at common output terminal(s). In general, each output line from one DAC is connected to a corresponding output line of the other DAC. Regardless of which of the common nodes is analogized to applicant's output node(s), *all of Westra's DACs are coupled to Westra's output node(s) at any given time.* (Westra, Figs. 1, 3). Westra does not teach or suggest coupling only one of the first and second DACs to an output node at any given time.

Thus applicant respectfully submits *none of the Examiner's cited references, alone or in combination, teaches or suggests switch circuitry coupling the differential output of at most a selected one of the first and second DACs to a pair of switch nodes, wherein the differential output of a non-selected one of the first and second DACs is shorted.*

In contrast, claim 1 includes the language:

> 1. An apparatus for performing digital-to-analog conversion, comprising:
> first and second current steering digital-to-analog converters (DAC), each DAC having a first and second output forming a differential DAC output; and
> *switch circuitry, wherein the switch circuitry couples the differential output of at most a selected one of the first and second DACs to a pair of switch nodes, wherein the differential output of a non-selected one of the first and second DACs is shorted.*

(Claim 1)(*emphasis added*)

Thus applicant respectfully submits claim 1 is patentable under 35 U.S.C. § 103 in view of the cited references. Given that claims 2-10 depend from claim 1, applicant respectfully submits claims 2-10 are likewise patentable over the cited references.

Applicant respectfully submits the rejections under 35 U.S.C. § 103 have been overcome.

Conclusion

In view of the amendments and arguments presented above, applicant respectfully submits the applicable rejections and objections have been overcome. Accordingly, all of claims 1-20 should be found to be in condition for allowance.

If there are any issues that can be resolved by telephone conference, the Examiner is respectfully requested to contact the undersigned at **(512) 858-9910**.

Respectfully submitted,

Date September 17, 2004 William D. Davis

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